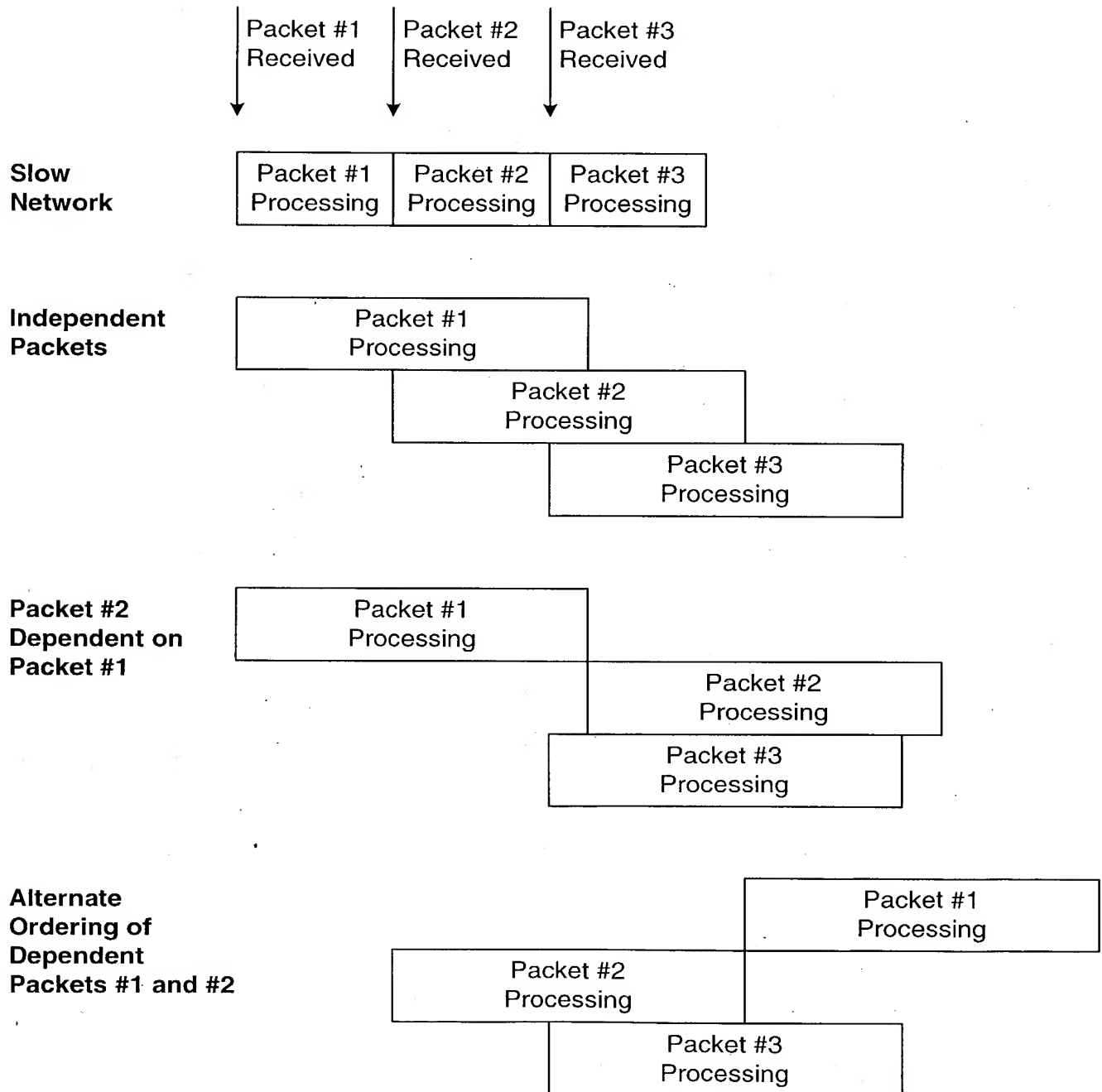
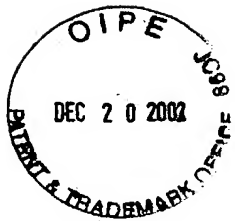




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Figure 1
General Packet Processing Examples

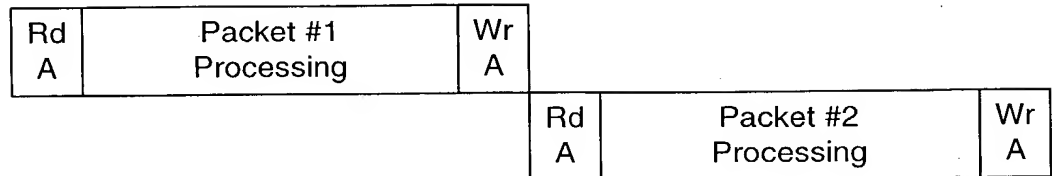




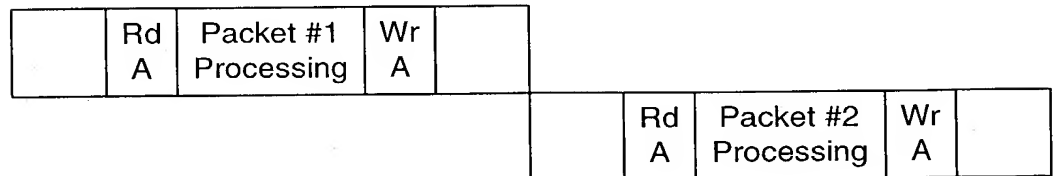
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Figure 2
Optimal Overlap of Dependent Packets

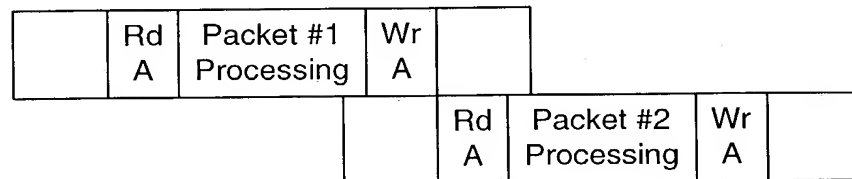
**No Overlap
Possible**



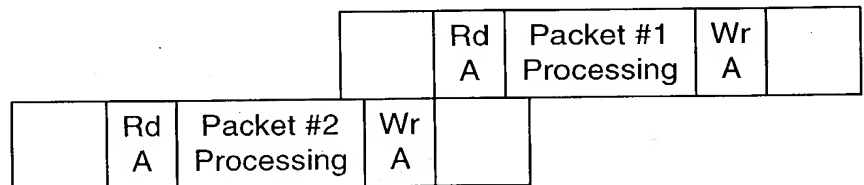
**Non-Optimal
Overlap**



**Optimal
Overlap**



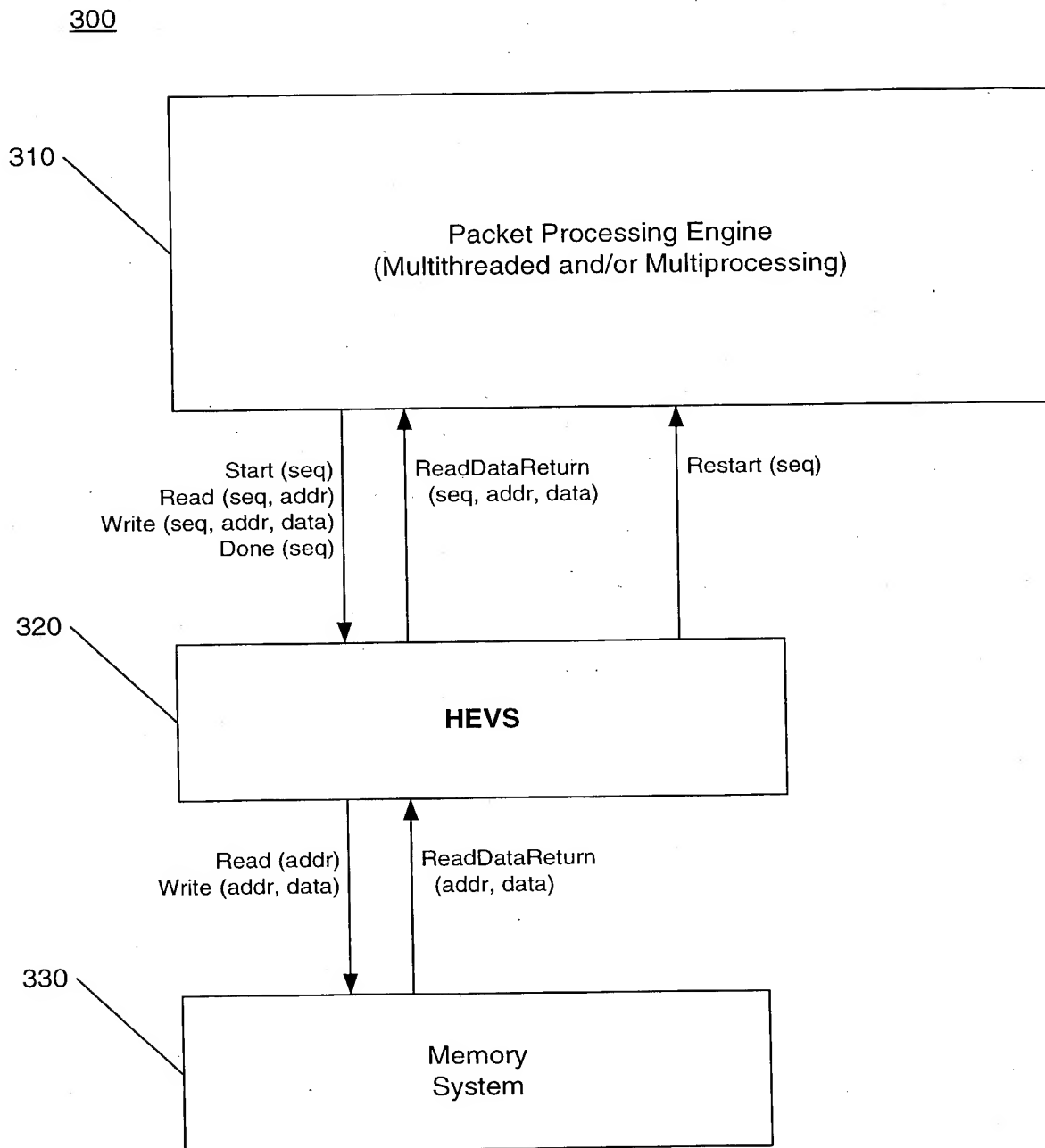
**Alternate
Ordering
Optimal
Overlap**





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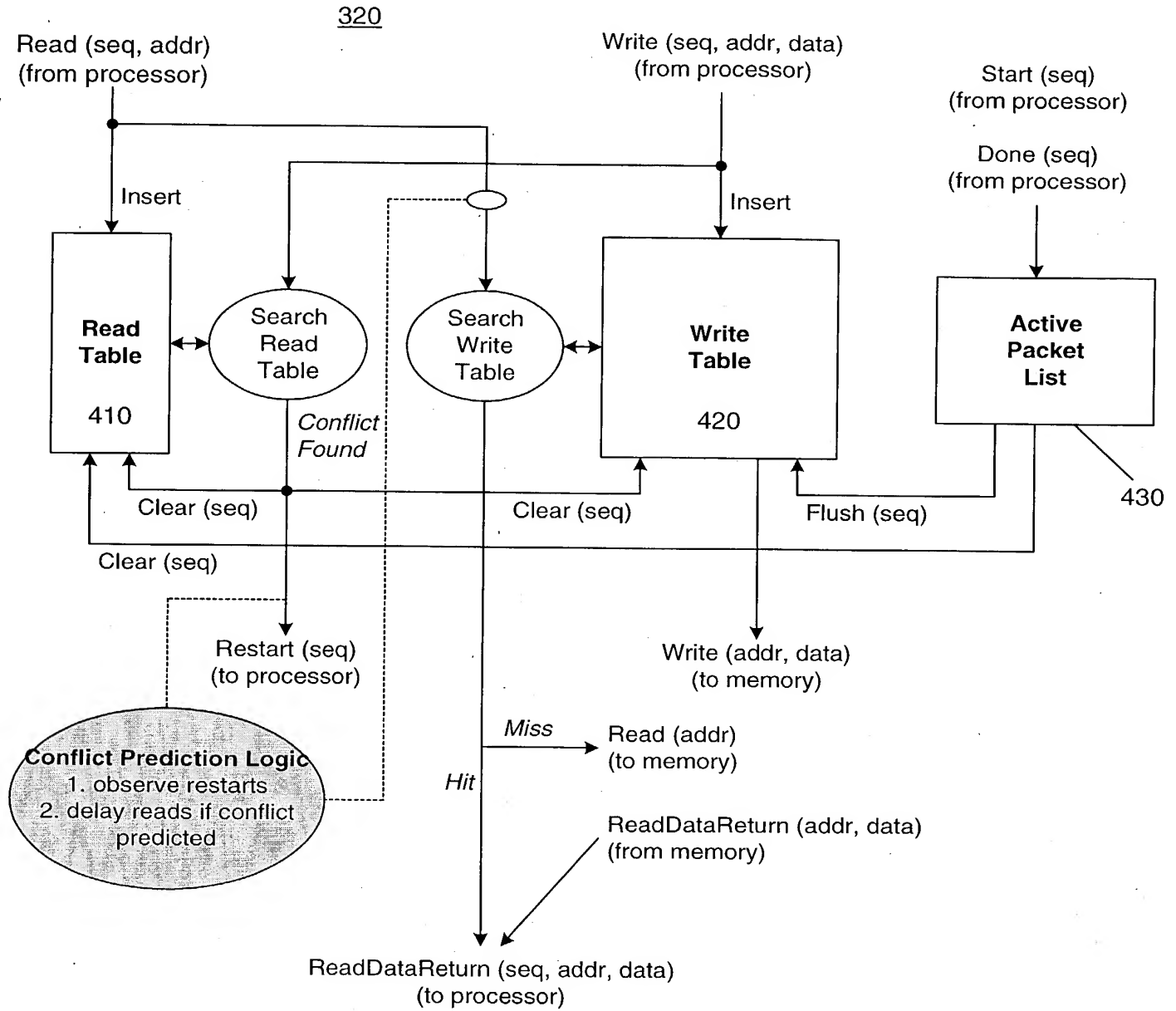
Figure 3
Hardware Enforced Virtual Sequentiality Block Diagram





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Figure 4
Hardware Enforced Virtual Sequentiality Mechanism





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Figure 5
Read Table and Write Table Detail

Read Table			Write Table				
410	Seq.	Addr.	Seq.	Addr.	Data	Depend	420
p: q: s: t:							
	1	A					
	2	B					
	3	B					
	2	A					

r:	2	B	X	3
u:	1	A	X	(null)

Time Sequence:

1. Packet #1 reads location A
Entry **p:** created in Read Table
Write Table is searched, no matches found so memory read is performed
2. Packet #2 reads location B
Entry **q:** created in Read Table
Write Table is searched, no matches found so memory read is performed
3. Packet #2 writes location B
Entry **r:** created in Write Table
Read Table is searched, no conflicts found
4. Packet #3 reads location B
Entry **s:** created in Read Table
Write Table is searched, entry **r:** found, data X forwarded and dependency list updated
5. Packet #2 reads location A
Entry **t:** created in Read Table
Write Table is searched, no matches found so memory read is performed
6. Packet #1 writes location A
Entry **u:** created in Write Table
Read Table is searched for newer sequence read, entry **t:** is found
Conflict is signaled to processor, Packet #2 is restarted
Entry **q:** and all other sequence 2 entries are deleted
Deletion of entry **r:** triggers Packet #3 restart signaled



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Figure 6
Conflict Detection Processing Examples

